#### **SPECIFICATIONS**

# PXIe-5162

# PXIe, 1.5 GHz, 5 GS/s, 10-Bit PXI Express Oscilloscope

# Contents

Definitions	2
Conditions.	
Vertical	3
Analog Input	
Impedance and Coupling	
Voltage Levels	
Accuracy	
Bandwidth and Transient Response	
Spectral Characteristics.	
Horizontal	
Sample Clock	12
Phase-Locked Loop (PLL) Reference Clock	14
External Sample Clock (CLK IN, Front Panel Connector)	15
External Reference Clock In (CLK IN, Front Panel Connector)	
Reference Clock Out (CLK OUT, Front Panel Connector)	
Trigger	16
Analog Trigger (Edge Trigger Type)	
External Trigger (TRIG, Front Panel Connector).	
Digital Trigger (Digital Trigger Type)	17
Programmable Function Interface (PFI 0 and PFI 1, Front Panel Connectors)	
CableSense	18
Waveform Specifications	19
Memory Sanitization	19
Calibration	19
External Calibration	19
Self-Calibration	19
Calibration Specifications	19
Software	20
Driver Software	20
Application Software	20
Interactive Soft Front Panel and Configuration	20
TClk Specifications	20
Power Requirements	21
Physical Characteristics	21



Environmental Characteristics.	. 22
Product Certifications and Declarations	. 22

### **Definitions**

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design, or verified during production and calibration.

*Characteristics* describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- Typical specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- Measured (meas) specifications describe the measured performance of a representative model.

Specifications are *Typical* unless otherwise noted.

## **Conditions**

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges
- All bandwidths and bandwidth limit filters
- Sample rate set to 1.25 GS/s, 2.5 GS/s, or 5 GS/s
- Onboard Sample clock locked to onboard Reference clock

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature ranges of 0 °C to 45 °C
- The PXIe-5162 is warmed up for 15 minutes at ambient temperature
- Self-calibration is completed after warm-up period
- Calibration cycle is maintained
- The PXI Express chassis fan speed is set to HIGH, the foam fan filters are removed if
  present, and the empty slots contain PXI chassis slot blockers and filler panels. For more
  information about cooling, refer to the Maintain Forced-Air Cooling Note to Users
  document available at ni com/manuals.
- NI-SCOPE 4.1 or later instrument driver is used
- External calibration is performed at 23 °C  $\pm$  3 °C

Typical specifications are valid under the following conditions unless otherwise noted:

• Ambient temperature ranges of 0 °C to 45 °C

# Vertical

# **Analog Input**

Number of channels	
PXIe-5162 (2 CH)	Two (simultaneously sampled)
PXIe-5162 (4 CH)	Four (simultaneously sampled)
Input type	Referenced single-ended
Connectors	BNC

# Impedance and Coupling



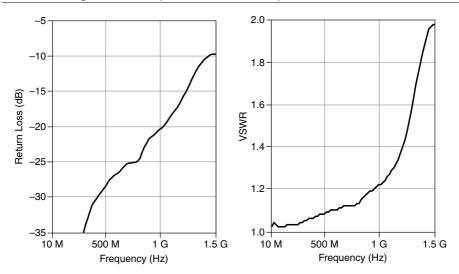
**Note** Impedance and coupling are software-selectable on a per-channel basis.

Table 1. Input Impedance

Impedance Setting	Typical	Warranted
50 Ω	$50~\Omega \pm 1.50\%$	$50 \Omega \pm 1.75\%$
1 ΜΩ	$1~\text{M}\Omega \pm 0.75\%$	$1~\text{M}\Omega \pm 0.90\%$

Input capacitance <sup>1</sup>	15 pF $\pm$ 0.8 pF, nominal 15 pF $\pm$ 2.5 pF, warranted
Input coupling	AC, DC

<sup>&</sup>lt;sup>1</sup> 1 M $\Omega$  input only.



# Voltage Levels

**Table 2.** 50  $\Omega$  Full-Scale (FS) Input Range and Vertical Offset Range

Input Range (V <sub>pk-pk</sub> )	Vertical Offset Range (V)
0.05 V	±0.5
0.1 V	±0.5
0.2 V	±0.5
0.5 V	±0.5
1 V	±0.5
2 V	±1.5
5 V	0

**Table 3.** 1 M $\Omega$  FS Input Range and Vertical Offset Range

Input Range (V <sub>pk-pk</sub> )	Vertical Offset Range (V)
0.05 V	±0.5
0.1 V	±0.5

**Table 3.** 1 MΩ FS Input Range and Vertical Offset Range (Continued)

Input Range (V <sub>pk-pk</sub> )	Vertical Offset Range (V)
0.2 V	±0.5
0.5 V	±0.5
1 V	±0.5
2 V	±5
5 V	±5
10 V	±5
20 V	±30
50 V	±15

#### Maximum input overload<sup>2</sup>

50 Ω	Peaks  ≤5 V, nominal
1 ΜΩ	Peaks  ≤42 V, nominal

## Accuracy

Resolution	10 bits
DC accuracy <sup>3</sup>	$ \begin{array}{l} \pm [(2\% \times   Reading - Vertical \ Offset  ) \\ + (1.4\% \times   Vertical \ Offset  ) \\ + (0.6\% \ of \ FS) + 600 \ \mu V] \end{array} $
DC drift <sup>4</sup>	$\pm[(0.1\% \times  Reading - Vertical Offset ) + (0.025\% \times  Vertical Offset ) + (0.03\% of FS)] per °C, nominal$
AC amplitude accuracy <sup>3</sup>	±0.5 dB at 50 kHz
AC amplitude drift <sup>4</sup>	±0.01 dB per °C at 50 kHz, nominal

<sup>&</sup>lt;sup>2</sup> Signals exceeding the maximum input overload may cause damage to the device.

<sup>&</sup>lt;sup>3</sup> Within ±3 °C of self-calibration temperature. This specification is *typical* for peak-to-peak input ranges of 0.05 V to 0.1 V and warranted for all other input ranges.

 $<sup>^4~</sup>$  Used to calculate errors when onboard temperature changes more than  $\pm 3~^{\circ}\mathrm{C}$  from the selfcalibration temperature.

Table 4. Channel-to-Channel Crosstalk, Nominal<sup>5</sup>

Input Impedance	Input Frequency	Crosstalk
	DC ≤ <i>f</i> ≤ 100 MHz	-60 dB
50 Ω	100 MHz < <i>f</i> ≤ 700 MHz	-45 dB
	700 MHz < <i>f</i> ≤ 1000 MHz	-40 dB
$1~\mathrm{M}\Omega^6$	DC ≤ <i>f</i> ≤ 100 MHz	-55 dB
	100 MHz < <i>f</i> ≤ 200 MHz	-45 dB

## Bandwidth and Transient Response

50 Ω bandwidth  $(-3 dB)^7$ 

1.5 GHz, warranted

**Table 5.** 1 M $\Omega$  Bandwidth (-3 dB)<sup>11</sup>

Input Impedance	Input Range (V <sub>pk-pk</sub> )	Nominal	Warranted
	0.05 V to 1 V	_	300 MHz
$1~\mathrm{M}\Omega^9$	2 V to 10 V	300 MHz	250 MHz <sup>10</sup>
	20 V to 50 V	300 MHz	_

Bandwidth-limiting filters	20 MHz
	175 MHz
Rise/fall time <sup>12</sup>	
50 Ω	320 ps
$1~\mathrm{M}\Omega^{13}$	1.4 ns

Measured on one channel with test signal applied to another channel with the same range setting on both channels.

<sup>&</sup>lt;sup>6</sup> Only valid on peak-to-peak input ranges of 0.05 V to 10 V.

<sup>&</sup>lt;sup>7</sup> Normalized to 50 kHz.

<sup>&</sup>lt;sup>8</sup> For ambient temperature ranges of 0 °C to 30 °C

<sup>&</sup>lt;sup>9</sup> Verified using a 50  $\Omega$  source and 50  $\Omega$  feed-through terminator.

<sup>&</sup>lt;sup>10</sup> For ambient temperature ranges of 0 °C to 30 °C

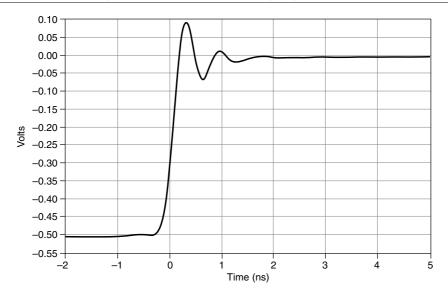
<sup>&</sup>lt;sup>11</sup> Normalized to 50 kHz.

<sup>&</sup>lt;sup>12</sup> 50% FS input pulse.

Verified using a 50  $\Omega$  source and 50  $\Omega$  feed-through terminator.

$50~\Omega^{15}$	170 kHz
$1~\mathrm{M}\Omega$	17 Hz

Figure 2. PXIe-5162 Step Response, 50  $\Omega$ , 1  $V_{pk-pk}$  Input Range, -0.25 V Programmable Offset, 150 ps Rising Edge, Measured



 $<sup>^{14}</sup>$   $\,$  Verified using a 50  $\Omega$  source.

With AC coupling enabled, the DC resistance to ground is 20 k $\Omega$ .

**Figure 3.** PXIe-5162 Step Response, 1 MΩ, 1  $V_{pk-pk}$  Input Range, -0.25 V Programmable Offset, 500 ps Rising Edge, Measured<sup>16</sup>

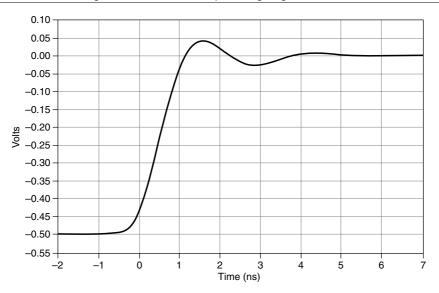
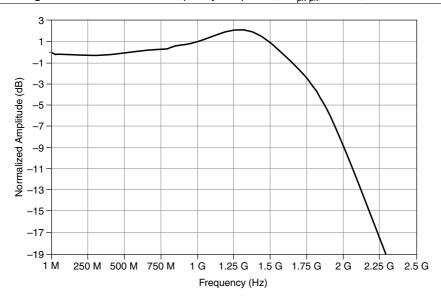


Figure 4. PXIe-5162 50  $\Omega$  Frequency Response, 1  $V_{pk-pk}$ , 5 GS/s, Measured



 $<sup>^{16}</sup>$   $\,$  Verified using a 50  $\Omega$  source and 50  $\Omega$  feed-through terminator.

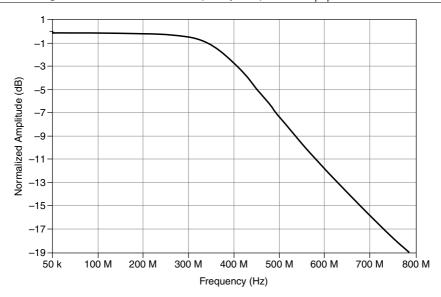
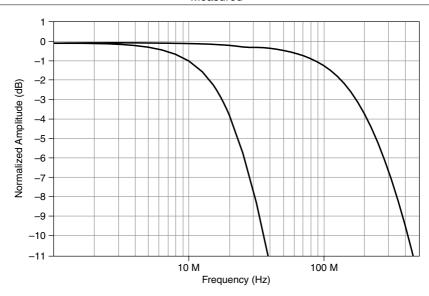


Figure 6. PXIe-5162 Bandwidth-Limiting Filters Frequency Response, 1 V<sub>pk-pk</sub>, Measured



 $<sup>^{17}</sup>$  Verified using a 50  $\Omega$  source and 50  $\Omega$  feed-through terminator.

# **Spectral Characteristics**

### 50 Ω Spectral Characteristics

Table 6. Spurious-Free Dynamic Range (SFDR), Measured<sup>18</sup>

		SFDR	
Input Frequency	Input Range (V <sub>pk-pk</sub> )	1.25 GS/s, 2.5 GS/s <sup>19</sup> , 5.0 GS/s <sup>19</sup>	2.5 GS/s, 5.0 GS/s
	0.05 V	52 dBc	40 dBc
<10 MHz	0.1 V	52 dBc	46 dBc
~10 WHZ	0.2 V	56 dBc	46 dBc
	0.5 V to 5 V	56 dBc	50 dBc
≥10 MHz to ≤1 GHz	0.05 V	46 dBc	40 dBc
≥10 MHZ t0 ≤1 GHZ	0.1 V to 5 V	46 dBc	46 dBc

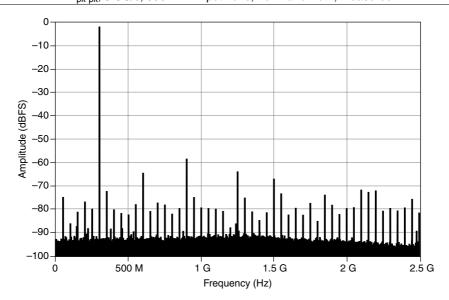
Table 7. Effective Number of Bits (ENOB), Nominal<sup>18</sup>

Input Frequency	Input Range (V <sub>pk-pk</sub> )	ENOB
	0.05 V	6.0
<1 GHz	0.1 V	6.6
	0.2 V to 5 V	7.0

 $<sup>^{18}\,</sup>$  -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics. 7.2 kHz resolution bandwidth.

<sup>19</sup> Excludes ADC interleaving spurs.

Figure 7. PXIe-5162 Single-Tone Spectrum, 2.98 dBm Input Signal at Connector, 50  $\Omega$ , 1 V<sub>pk-pk</sub>, 5 GS/s, 300 MHz Input Tone, Full Bandwidth, Measured



## 1 MΩ Spectral Characteristics<sup>20</sup>

Table 8. SFDR, Nominal<sup>21</sup>

		SFDF	1
Input Frequency	Input Range (V <sub>pk-pk</sub> )	1.25 GS/s, 2.5 GS/s <sup>22</sup> , 5.0 GS/s <sup>22</sup>	2.5 GS/s, 5.0 GS/s
<10 MHz	0.05 V to 10 V	53 dBc	48 dBc
<10 MHz	20 V	50 dBc	44 dBc
≥10 MHz to ≤100 MHz	0.05 V to 0.5 V	53 dBc	48 dBc
≥10 WITZ tO ≥100 WITZ	1 V to 5 V	48 dBc	48 dBc

 $<sup>^{20}~</sup>$  Verified using a 50  $\Omega$  source and 50  $\Omega$  feedthrough terminator.

<sup>&</sup>lt;sup>21</sup> -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics. 7.2 kHz resolution bandwidth.

<sup>&</sup>lt;sup>22</sup> Excludes ADC interleaving spurs.

Table 9. ENOB, Nominal<sup>21</sup>

Input Frequency	Input Range (V <sub>pk-pk</sub> )	ENOB
<10 MHz	10 V to 20 V	7.1
	0.05 V	6.2
≤100 MHz	0.1 V	6.8
	0.2 V to 5 V	7.1

#### Noise

Table 10. RMS Noise<sup>23</sup>

Input Impedance	Input Range (V <sub>pk-pk</sub> )	Typical	Warranted
	0.05 V	0.55% of FS	0.62% of FS
$50~\Omega$	0.1 V	0.33% of FS	0.39% of FS
	0.2 V to 5 V	0.28% of FS	0.34% of FS
	0.05 V	0.55% of FS	0.62% of FS
$1~\mathrm{M}\Omega$	0.1 V	0.33% of FS	0.39% of FS
	0.2 V to 50 V	0.28% of FS	0.34% of FS

### Skew

Channel-to-channel skew	
$50~\Omega$ to $50~\Omega$	<25 ps, nominal
1 M $\Omega$ to 1 M $\Omega$	<125 ps, nominal
$50~\Omega$ to $1~M\Omega$	<800 ps, nominal

# Horizontal

# Sample Clock

Sources	
Internal	Onboard clock (internal VCO)
External	Front panel SMB connector

 $<sup>^{23}</sup>$   $\,$  Verified using a 50  $\Omega$  terminator connected to input.

#### **Onboard Clock**

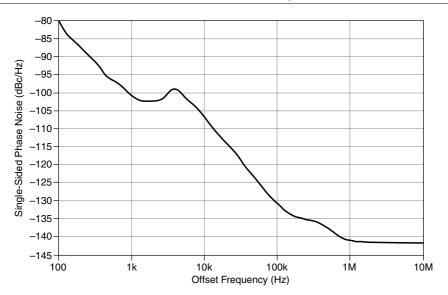
Real-time sample rate range <sup>24</sup>	
One channel enabled	76.299 kS/s to 5 GS/s
Two channels enabled <sup>25</sup>	76.299 kS/s to 2.5 GS/s
Four channels enabled	76.299 kS/s to 1.25 GS/s
Random interleaved sampling (RIS) range <sup>26</sup>	Up to 100 GS/s

Divide by n decimation from 1.25 GS/s used for all rates less than 1.25 GS/s. For more information about the Sample Clock and decimation, refer to the NI High-Speed Digitizers Help.

<sup>&</sup>lt;sup>25</sup> For the PXIe-5162 (4 CH), supported on channels 0 and 2. For the PXIe-5162 (2 CH), supported on channels 0 and 1.

 $<sup>^{26}</sup>$  With one channel enabled, stepped in multiples of 5 GS/s. With two channels enabled, stepped in multiples of 2.5 GS/s. With four channels enabled, stepped in multiples of 1.25 GS/s.

**Figure 8.** PXIe-5162 Phase Noise (Plotted without Spurs) at 1 GHz, 3 dBm Input Signal, Locked to Onboard Reference Clock, Measured



Sample Clock jitter <sup>27</sup>	180 fs RMS (12 kHz to 10 MHz), nominal
Timebase frequency	2.5 GHz
Timebase accuracy <sup>28</sup>	±10 ppm, typical ±25 ppm, warranted

# Phase-Locked Loop (PLL) Reference Clock

Internal	Onboard 10 MHz reference
External	External 10 MHz (front panel CLK IN connector) or PXI_CLK10 (backplane connector)
aty cycle tolerance	45% to 55%

<sup>27</sup> Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

When phase-locked to an external Reference Clock, the timebase accuracy is equal to the external Reference Clock accuracy. For example, when locked to the System Reference Clock of a PXI Express chassis, the module inherits the accuracy of the chassis System Reference Clock.

# External Sample Clock (CLK IN, Front Panel Connector)

Input voltage range, when configured as a Sample Clock	-10 dBm through 16 dBm
Maximum input overload, when configured as a Sample Clock	18 dBm
Impedance	50 Ω
Coupling	AC
Frequency range	1.25 GHz to 2.5 GHz <sup>29</sup>

# External Reference Clock In (CLK IN, Front Panel Connector)

Input voltage range, when configured as a Reference Clock	$200 \text{ mV}_{pk\text{-}pk}$ to $4 \text{ V}_{pk\text{-}pk}$
Maximum input overload, when configured as a Reference Clock	5 $V_{pk-pk}$ with $ Peaks  \le 10 \text{ V}$
Impedance	50 Ω
Coupling	AC
Frequency range <sup>30</sup>	10 MHz

# Reference Clock Out (CLK OUT, Front Panel Connector)

Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	±10 mA

<sup>&</sup>lt;sup>29</sup> To achieve the same real-time sample rate ranges as the onboard clock, a 2.5 GHz frequency is

The PLL Reference Clock frequency must be accurate to ±25 ppm.

# Trigger

Supported trigger	Reference (Stop) Trigger
Trigger types	Edge Digital Immediate Hysteresis Software
Trigger sources	
PXIe-5162 (2 CH)	CH 0, CH 1, TRIG, PFI 0, PFI 1, PXI_TRIG <06>, and Software
PXIe-5162 (4 CH)	CH 0, CH 1, CH 2, CH 3, PFI 0, PFI 1, PXI_TRIG <06>, and Software
Time-to-digital conversion circuit time resolution	4 ps
Dead time	710 ns, nominal
Holdoff	6.4 ns to 27.4 s
Trigger delay	From 0 to 73,786,976 seconds (28 months), nominal

# Analog Trigger (Edge Trigger Type)

Sources	
PXIe-5162 (2 CH)	CH 0, CH 1, or TRIG <sup>31</sup>
PXIe-5162 (4 CH)	CH 0, CH 1, CH 2, or CH 3
Trigger filters	
Low-frequency reject	150 kHz, nominal
High-frequency reject	150 kHz, nominal
Trigger sensitivity	3% of FS at ≤100 MHz, nominal
Trigger accuracy <sup>32</sup>	6% of FS at ≤100 MHz, nominal
Trigger jitter	4.7 ps

<sup>31</sup> For specifications on the TRIG input, refer to the External Trigger (TRIG, Front Panel Connector) section.

<sup>32</sup> When the impedance settings of the triggering input and the analog input channel are the same. Delay will increase if the impedance of the triggering input does not match the impedance of the analog input channel.

## External Trigger (TRIG, Front Panel Connector)



Note TRIG is valid only for the PXIe-5162 (2 CH) device.

Connector	BNC
Impedance	$50~\Omega$ or $1~\text{M}\Omega$
Coupling	AC or DC
Input voltage range	
50 Ω	±2.5 V
1 ΜΩ	±5 V
Maximum input overload	
50 Ω	Peaks  ≤5 V, nominal
1 ΜΩ	Peaks  ≤42 V, nominal
Trigger sensitivity	3% of FS at ≤100 MHz, nominal
Trigger accuracy <sup>33</sup>	8% of FS at ≤100 MHz, nominal
Trigger jitter	4.7 ps

# Digital Trigger (Digital Trigger Type)

Sources <sup>34</sup>	
Front panel SMB connector	PFI <01>
Backplane connector	PXI_TRIG <06>

# Programmable Function Interface (PFI 0 and PFI 1, Front Panel Connectors)

Connector	SMB jack
Direction	Bidirectional

When the impedance settings of the triggering input and the analog input channel are the same. Delay will increase if the impedance of the triggering input does not match the impedance of the analog input channel.

<sup>&</sup>lt;sup>34</sup> Subsample trigger accuracy not supported on PFI 1 or PXI\_TRIG<0..6>.

#### As an Input (Trigger)

Destinations	Start Trigger (Acquisition Arm) Reference (Stop) Trigger Advance Trigger
Input impedance	10 kΩ
$V_{\mathrm{IH}}$	2.0 V
$V_{\mathrm{IL}}$	0.8 V
Maximum input overload	-0.5 V to 5.5 V
Maximum frequency	25 MHz

#### As an Output (Event)

Sources	Ready for Start
	Start Trigger (Acquisition Arm)
	Ready for Reference
	Arm Reference Trigger
	Reference (Stop) Trigger
	End of Record
	Ready for Advance
	Advance Trigger
	Done (End of Acquisition)
	Probe Compensation <sup>35</sup>
Output impedance	50 Ω, nominal
Logic type	3.3 V CMOS
Maximum current drive	±10 mA
Maximum frequency	25 MHz

## CableSense

CableSense pulse voltage <sup>36</sup>	0.5 V, nominal
CableSense pulse rise time <sup>37</sup>	650 ps, nominal

Driver support for CableSense on the PXIe-5162 was first available in NI-SCOPE 18.7.

#### **Related Information**

For more information about CableSense technology, refer to ni.com/cablesense.

<sup>&</sup>lt;sup>35</sup> 1 kHz, 50% duty cycle square wave, PFI 1 only.

<sup>&</sup>lt;sup>36</sup> When measured with a high-impedance device.

When sourcing into a 50  $\Omega$  cable or load.

# Waveform Specifications

Onboard memory sizes <sup>38</sup>	64 MB or 2 GB
Minimum record length	1 sample
Number of pretrigger samples <sup>39</sup>	Zero up to full record length
Number of posttrigger samples <sup>39</sup>	Zero up to full record length
Maximum number of records in onboard n	nemory <sup>40</sup>
64 MB	65,536
2 GB	100,000
Allocated onboard memory per record	[(Record length + 448 samples) × 2 bytes/sample], rounded up to an integer multiple of 128 bytes (minimum 512 bytes)

# **Memory Sanitization**

For information about memory sanitization, refer to the letter of volatility for your device, which is available at *ni.com/manuals*.

### Calibration

#### **External Calibration**

External calibration calibrates the onboard references used in self-calibration and the external trigger levels. All calibration constants are stored in nonvolatile memory.

#### Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, triggering, and timing errors for all input ranges.

# Calibration Specifications

Interval for external calibration	2 years
Warm-up time	15 minutes

<sup>&</sup>lt;sup>38</sup> Onboard memory is shared among all enabled channels. Devices with NI part number 154772Ax2L had 1 GB of onboard memory.

<sup>&</sup>lt;sup>39</sup> Single-record and multirecord acquisitions.

<sup>&</sup>lt;sup>40</sup> You can exceed these numbers if you fetch records while acquiring data. For more information, refer to the NI High-Speed Digitizers Help.

### Software

#### **Driver Software**

Driver support for this device was first available in NI-SCOPE 4.1.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-5162. NI-SCOPE provides application programming interfaces for many development environments.

## **Application Software**

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows<sup>TM</sup>/CVI<sup>TM</sup>
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

## Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PXIe-5162 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.



**Note** InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PXIe-5162 was first available via InstrumentStudio in NI-SCOPE 18.1 and via the NI-SCOPE SFP in NI-SCOPE 4.1. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5162. MAX is included on the driver media.

## **TClk Specifications**

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help*, which is located within the *NI High-Speed Digitizers Help*. For other configurations, including multichassis systems, contact NI Technical Support at *ni.com/support*.

#### Intermodule SMC Synchronization Using NI-TClk for Identical Modules

Specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample clocks of each module.
- All parameters are set to identical values for each SMC-based module.
- Modules are synchronized without using an external Sample clock.
- Self-calibration is completed.



**Note** Although you can use NI-TClk to synchronize non-identical SMC-based modules, these specifications apply only to synchronizing identical modules.

Skew <sup>41</sup>	100 ps, nominal
Skew after manual adjustment	≤5 ps, nominal
Sample clock delay/adjustment resolution	20 fs

#### **Related Information**

NI-TClk Overview

For more information on manual adjustment, refer to NI-TClk Manual Calibration on NI-SCOPE Devices.

## **Power Requirements**

+3.3 VDC	2.2 A, nominal
+12 VDC	2.3 A, nominal
Total power	34.8 W, nominal

# Physical Characteristics

Dimensions	3U, 1 slot, PXI Express gen 1 x4 Module 21.4 cm × 2.0 cm × 13.1 cm
	$(8.4 \text{ in.} \times 0.8 \text{ in.} \times 5.1 \text{ in.})$
Weight	430 g (15 oz.)

<sup>&</sup>lt;sup>41</sup> Caused by clock and analog path delay differences. No manual adjustment performed. Tested with a NI PXIe-1082 chassis with a maximum slot-to-slot skew of 100 ps.

### **Environmental Characteristics**

Temperature	
Operating	0 °C to 45 °C
Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature
Shock and Vibration	
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g RMS
Non-operating	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

### **Product Certifications and Declarations**

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit *ni.com/certification*, search by model number or product line, and click the appropriate link in the Certification column.

Information is subject to change without notice. Refer to the *NI Trademarks and Logo Guidelines* at ni.com/trademarks for information on NI trademarks. Other product and company names mentioned herein are trademarks or trade names of their respective companies. For patents covering NI products/technology, refer to the appropriate location: Help»Patents in your software, the patents.txt file on your media, or the *National Instruments Patent Notice* at ni.com/patents. You can find information about end-user license agreements (EULAs) and third-party legal notices in the readme file for your NI product. Refer to the *Export Compliance Information* at ni.com/legal/export-compliance for the NI global trade compliance policy and how to obtain relevant HTS codes, ECCNs, and other import/export data. NI MAKES NO EXPRESS OR IMPLIED WARRANTIES AS TO THE ACCURACY OF THE INFORMATION CONTAINED HEREIN AND SHALL NOT BE LIABLE FOR ANY ERRORS. U.S. Government Customers: The data contained in this manual was developed at private expense and is subject to the applicable limited rights and restricted data rights as set forth in FAR 52.227-14, DFAR 252.227-7014, and DFAR 252.227-7015.